



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Cheng, *et al.*

Docket No.: TSM03-0698

Filed: 2/25/2004

Examiner: Kevin Quinto

Serial No.: 10/786,643

Art Unit: 2826

Title: CMOS Structure and Related Method

Mail Stop Amendment  
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Respectfully submitted,

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Applicant: Cheng, *et al.* Docket No.: TSM03-0698  
Serial No.: 10/786,643 Art Unit: 2826  
Filed: 02/25/2004 Examiner: Quinto, Kevin  
For: CMOS Structure and Related Method

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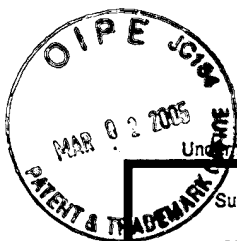
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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### Complete if Known

Application Number	10/786,643
Filing Date	2/25/2004
First Named Inventor	Cheng, et al.
Art Unit	2826
Examiner Name	Quinto, Kevin
Attorney Docket Number	TSM03-0698

Sheet	1	of	6
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### U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
	1	US-4,069,094	01-17-1978	Shaw et al.	
	2	US-4,314,269	02-02-1982	Fujiki	
	3	US-4,497,683	02-05-1985	Celler et al.	
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				Art Unit	2826
Examiner Name	Quinto, Kevin				
Attorney Docket Number	TSM03-0698				
Sheet	2	of	6		

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	41	US-2002/0140031 A1	10-03-2002	Rim	
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Examiner Name	Quinto, Kevin				
Sheet	3	of	6	Attorney Docket Number	TSM03-0698

FOREIGN PATENT DOCUMENTS						
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		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				
	76	EP 0 683 522 A2	11-22-1995	International Business Machines Corporation		
	77	EP 0 828 296 A2	03-11-1998	International Business Machines Corporation		
	78	WO 03/017336 A2	02-27-2003	Amberwave Systems Corporation		

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	79	"Future Gate Stack," International Sematech, 2001 Annual Report.	
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of

6

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Application Number 10/786,643

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First Named Inventor Cheng, et al.

Art Unit 2826

Examiner Name Quinto, Kevin

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	83	CHANG, L., et al., "Direct-Tunneling Gate Leakage Current in Double-Gate and Ultrathin Body MOSFETs," 2002 IEEE Transactions on Electron Devices, Vol. 49, No. 12, December 2002, pp. 2288-2295.	
	84	CHANG, L., et al., "Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs," IEEE, 2001, 4 pages.	
	85	GÁMIZ, F., et al., "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," Journal of Applied Physics, Vol. 92, No. 1, July 1, 2002, pp. 288-295.	
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	94	LEITZ, C.W., et al., "Hole Mobility Enhancements In Strained Si/Si <sub>1-y</sub> Ge <sub>y</sub> P-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown On Relaxed Si <sub>1-x</sub> Ge <sub>x</sub> (x<y) Virtual Substrates," Applied Physics Letters, Vol. 79, No. 25, December 17, 2001, pp. 4246-4248.	
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	102	NAYAK, D.K., et al., "Enhancement-Mode Quantum-Well Ge <sub>x</sub> Si <sub>1-x</sub> PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, April 1991, pp. 154-156.	
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				First Named Inventor	Cheng, et al.
				Art Unit	2826
				Examiner Name	Quinto, Kevin
Sheet	6	of	6	Attorney Docket Number	TSM03-0698

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	105	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.	
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	111	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM, 1992, pp. 1000-1002.	
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